## CLAIMS

What is claimed is:

1. A flipchip semiconductor package, comprising:

a first chip carrier accommodating at least one first chip having an active surface on which a plurality of solder bumps are formed for electrically connecting the first chip to the first chip carrier, and an opposing non-active surface;

a second chip carrier accommodating at least one second chip having an active surface on which a plurality of solder bumps are formed for electrically connecting the second chip to the second chip carrier, and an opposing non-active surface;

an adhesive layer, applied over the non-active surface of the fist chip allowing the second chip of the second chip carrier to be attached to the first chip of the first chip carrier;

a resin encapsulating layer, filled in between the first chip carrier and the second chip carrier for encapsulating the first chip, the second chip, and the plurality of solder bumps; and

a plurality of conductive through vias extending axially between the first chip carrier, the resin encapsulating layer, and the second chip carrier for electrically connecting the first chip to the first chip carrier via the second chip carrier and the conductive through vias.

2. The flipchip semiconductor package of claim 1, wherein a plurality of solder bumps are disposed on the exposed surface of the second chip carrier for forming electrical connection with another semiconductor package.

3. The flipchip semiconductor package of claim 1, wherein each of the first chip carrier and the second chip carrier is a substrate.

4. The flipchip semiconductor package of claim 1, wherein each of the first chip carrier and the second chip carrier is a tape carrier (TAB).

5. The flipchip semiconductor package of claim 1, wherein the adhesive layer is an insulating adhesive having high elasticity.
6. The flipchip semiconductor package of claim 1, wherein the resin encapsulating layer is made of resin materials having low hygrosocopicity and low viscosity.
7. A flip-chip semiconductor package, comprising:

a first chip carrier accommodating at least one first chip having an active surface on which a plurality of solder bumps are formed for electrically connecting the first chip to first chip carrier, and an opposing non-active surface;

a second chip carrier accommodating at least one second chip having an active surface on which a plurality of solder bumps are formed for electrically connecting the second chip to second chip carrier, and an opposing non-active surface;

an adhesive layer, applied over the non-active surface of the fist chip allowing the second chip of the second chip carrier to be attached to the first chip of the first chip carrier;

a resin encapsulating layer, filled in between the first chip carrier and the second chip carrier for encapsulating the first chip, the second chip, and the plurality of solder bumps; and

a plurality of conductive traces formed between the first chip carrier, the resin encapsulating layer, and the second chip carrier for electrically connecting the first chip to the first chip carrier via each of the conductive traces.
8. The flipchip semiconductor package of claim 7, wherein each of the first chip carrier and the second chip carrier is a substrate.
9. The flipchip semiconductor package of claim 7, wherein each of the first chip carrier and the second chip carrier is a tape carrier (TAB).
10. The flipchip semiconductor package of claim 7, wherein the adhesive layer is an insulating adhesive having high elasticity.

11. The flipchip semiconductor package of claim 7, wherein the resin encapsulating layer is made of resin materials having low hygrosocopicity and low viscosity.

12. The flipchip semiconductor package of claim 7, wherein the conductive traces have one end connected to the ball pads of the second chip carrier and the other end connected to the ball pads of the first chip carrier.